20–80nm Channel Length InGaAs Gate-all-around Nanowire MOSFETs with EOT=1.2nm and Lowest SS=63mV/dec

J. J. Gu,[1] X. W. Wang,[2] H. Wu,[1] J. Shao,[3] A. T. Neal,[1] M. J. Manfra,[3] R. G. Gordon,[2] and P. D. Ye[1]

[1] *School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47906, U.S.A.*

[2] *Department of Chemistry and Chemical Biology, Harvard University, Cambridge, MA 02138, U.S.A.*

[3] *Department of Physics, Purdue University, West Lafayette, IN, 47906, U.S.A.*

Tel: 1-765-494-7611, Fax: 1-765-496-7443, Email: yep@purdue.edu

Introduction: Recently, a top-down technology for III-V gate-all-around (GAA) nanowire MOSFETs has been demonstrated [1-2]. However, the device metrics such as g_m, V_{DD}, SS, DIBL, and the channel length (L_{ch}) scaling of the III-V GAA devices demonstrated in [1] are still greatly limited by the large EOT of the devices. In this abstract, we experimentally demonstrate InGaAs GAA nanowire MOSFETs with an EOT down to 1.2nm by the successful integration of complex oxide dielectric $LaAlO_3$ (k~16) [3]. The reduction of EOT has allowed the demonstration of the first 20nm L_{ch} InGaAs MOSFETs with g_m of 1.65mS/μm at V_{ds}=0.5V and negligible short channel effects (SCE). A systematic scaling metrics study with L_{ch} between 20-80nm and nanowire size-dependent transport study with nanowire width (W_{NW}) between 20-35nm has also been carried out for three different gate stacks, demonstrating near-ideal SS of 63mV/dec and DIBL of 7mV/V. It is shown that the integration of 4nm $LaAlO_3$ with ultra-thin 0.5nm Al_2O_3 interfacial layer allow reduction of EOT=1.2nm with optimized interface trap density (D_{it}), offering excellent scalability, near-ballistic transport, and high g_m at low supply voltage.

Experiments: Fig. 1 shows a schematic view of an InGaAs GAA nanowire MOSFET fabricated in this work. The starting material is a 30nm p-InGaAs channel layer, an 80nm undoped InP sacrificial layer, and a 100nm undoped InAlAs etch stop layer on semi-insulating InP substrate. The InGaAs channel layer consists of 10nm $In_{0.53}Ga_{0.47}As$ layer sandwiched by two 10nm $In_{0.65}Ga_{0.35}As$ layers to boost the channel mobility and reduce the D_{it}. Key device dimensions are shown in Fig. 1 and the process flow in Fig. 2. The L_{ch} is varied from 80nm down to 20nm, W_{NW} is varied from 35nm down to 20nm with a fixed nanowire height (H_{NW}) of 30nm. 4 parallel wires are integrated in each device. The three gate stacks studied are highlighted in Fig. 1-2. Samples A and B have a 0.5nm Al_2O_3/4nm $LaAlO_3$ stack (EOT=1.2nm), where Al_2O_3 was grown before $LaAlO_3$ for sample A and vise versa for sample B. Sample C has 3.5nm Al_2O_3 gate (EOT=1.7nm). Fig. 3 shows SEM images of the 20nm PMMA mask defining the smallest L_{ch} and a finished GAA device.

Results and discussion: Fig. 4-6 show the well-behaved output characteristics, transfer characteristics, and g_m-V_{gs} of a GAA FET (sample A) with L_{ch}=W_{NW}=20nm. The current is normalized by the total perimeter of the nanowire, i.e. W_G=2×(W_{NW}+H_{NW}). The 20nm L_{ch} device shows negligible channel length modulation, I_{ON}=850μA/μm at V_{dd}=0.8V, g_m of 1.65mS/μm at V_{ds}=0.5V, SS=75mV/dec and DIBL=40mV/V. The device operates in enhancement-mode with V_T=0.14V extracted by linear extrapolation at low V_{ds}. Fig. 7 shows the SS scaling metrics for sample A with W_{NW}=20nm. Error bars show the standard deviation of the measurement over 25 devices at each data point. Consistent sub-100mV/dec SS has been obtained for the devices at V_{ds}=0.5V for all L_{ch}. Figs. 8-9 show the SS and DIBL scaling metrics with different W_{NW}. No evident W_{NW} dependence is observed, indicating the current EOT and GAA structure yield a very small geometric screening length (λ) compared to L_{ch}. The mean SS and DIBL remain unchanged at ~75mV/dec and ~25mV/V with L_{ch} down to 50nm, showing the immunity of these devices to SCE. Fig. 10 shows the transfer characteristics of one of the three best devices with SS of 63mV/dec at V_{ds}=0.05V, indicating excellent gate control and low D_{it}. The lowest DIBL achieved is 7mV/V (not shown). Figs. 11-12 show that g_m and I_{ON} remain constant at small L_{ch} indicating near-ballistic transport. Fig. 13 shows the D_{it} box plot of sample A. The D_{it} is extracted from the SS at V_{ds}=0.05V for L_{ch}=50-80nm since these devices are immune to SCE. A mean D_{it} of ~4×10^{12} $eV^{-1}cm^{-2}$ is obtained with the lowest value of $9\times10^{11}eV^{-1}cm^{-2}$ corresponding to the 63mV/dec device. Fig. 14 shows the increasing g_m and I_{on} with decreasing W_{NW}, due to the quantum confinement and volume inversion effect [2]. Simulation of inversion charge distribution inside the InGaAs nanowires in Fig. 15 confirms volume inversion at all W_{NW}. Figs. 16-17 show the transfer characteristics and g_m-V_{gs} for 20nm L_{ch} InGaAs GAA MOSFETs with EOT=1.7nm (sample C). Increasing EOT has led to increased SCE, evident from the larger SS and DIBL. However, higher g_m=1.8mS/μm at V_{ds}=0.5V is obtained on sample C, indicating enhanced mobility with relaxed EOT. Fig. 18 shows the relatively low gate leakage current density for EOT=1.2 and 1.7nm even with the advanced 3D structure. Figs. 19-21 show the SS, DIBL, and V_T scaling metrics for sample A, B, and C. Sample C shows the largest SS and DIBL due to the larger EOT of 1.7nm. Sample B shows worse SS and DIBL compared to sample A with the same EOT=1.2nm due to the larger D_{it} [3]. This indicates that insertion of ultra-thin Al_2O_3 interfacial layer can improve complex oxide/InGaAs interface quality. Decreasing EOT also results in better V_T roll-off properties and is favorable for enhancement-mode operation. Fig. 22 benchmarks SS, DIBL in this work with InGaAs non-planar FETs fabricated in our group. Table 1 compares the device dimensions and performance in this work with non-planar and thin body planar InGaAs MOSFETs in the literature [4-8]. The successful demonstration of the smallest L_{ch}, W_{NW}, SS, DIBL and highest g_m has been achieved in this work.

Conclusions: We have demonstrated the shortest L_{ch}=20nm InGaAs GAA nanowire MOSFETs with ALD Al_2O_3/$LaAlO_3$ gate stack. Lowest SS of 63mV/dec and DIBL of 7mV/V have been achieved. Benefiting from both the ultimate scalability of GAA structure and excellent transport property of III-V channel, InGaAs GAA technology is a strong candidate for future high-speed low-power logic application.

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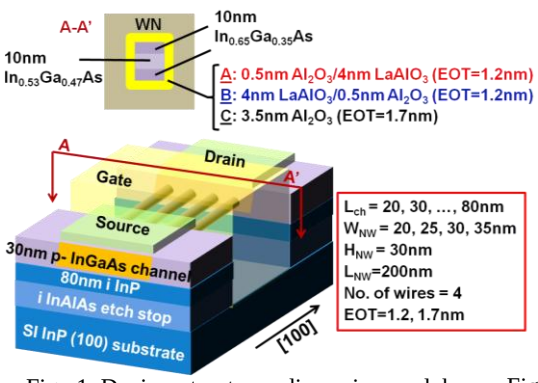


Fig. 1 Device structure, dimension and key parameters of InGaAs GAA MOSFETs.

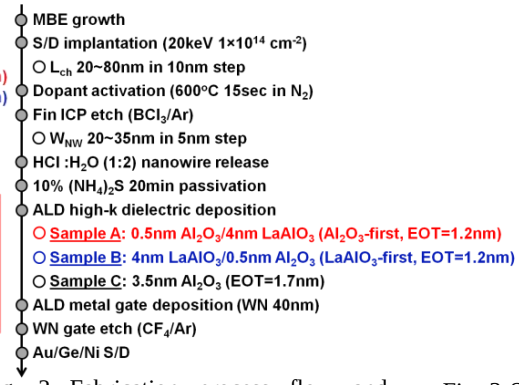


Fig. 2 Fabrication process flow and device splits of InGaAs GAA MOSFETs.

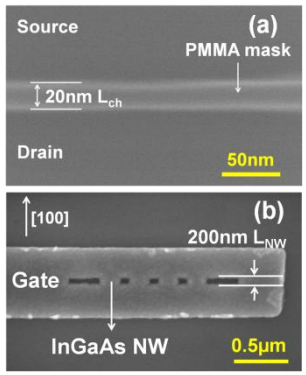


Fig. 3 SEM images of (a) PMMA mask defining 20nm L_{ch} (b) an InGaAs GAA FET with 4 wires.

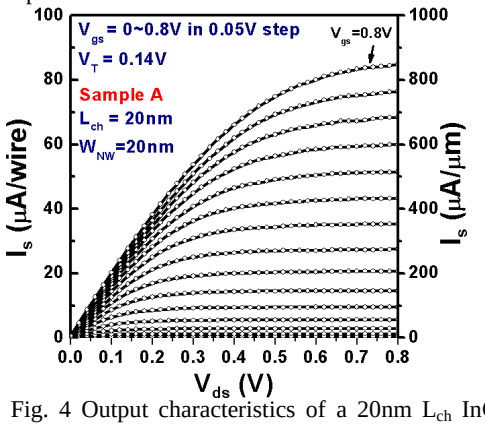


Fig. 4 Output characteristics of a 20nm L_{ch} InGaAs GAA MOSFET with Al_2O_3/$LaAlO_3$ gate dielectric (Sample A, EOT=1.2nm) and W_{NW}=20nm. I_s is used due to relatively large junction leakage current in I_d.

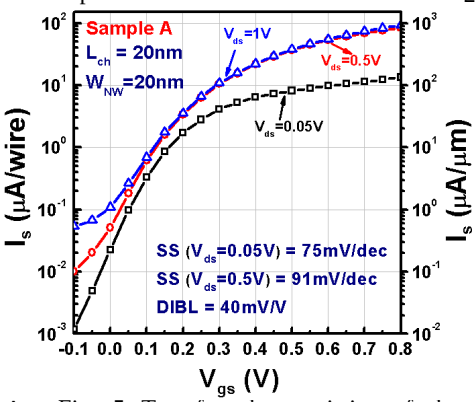


Fig. 5 Transfer characteristics of the same device shown in Fig. 4. W_G =100nm for W_{NW}=20nm normalized to perimeter.

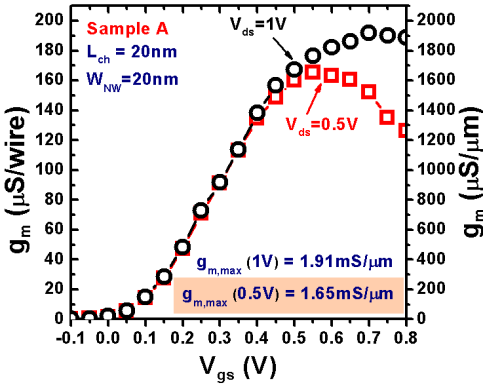


Fig. 6 Transconductance of the same device shown in Fig. 4.

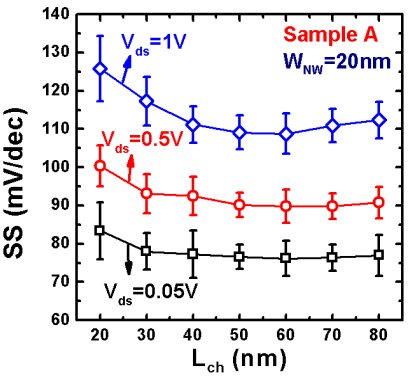


Fig. 7 SS scaling metrics for InGaAs GAA MOSFETs (Sample A, W_{NW}=20nm). Error bars show standard deviation of the measurements over 25 devices.

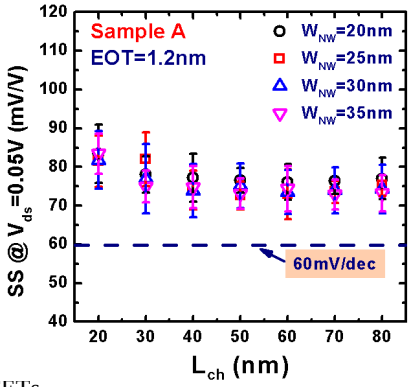


Fig. 8 SS (V_{ds}=0.05V) scaling metrics for sample A with W_{NW} from 20 to 35nm.

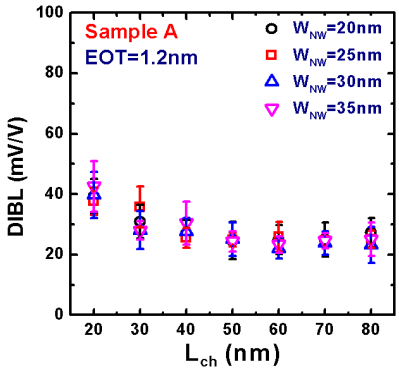


Fig. 9 DIBL scaling metrics for sample A with W_{NW} from 20 to 35nm.

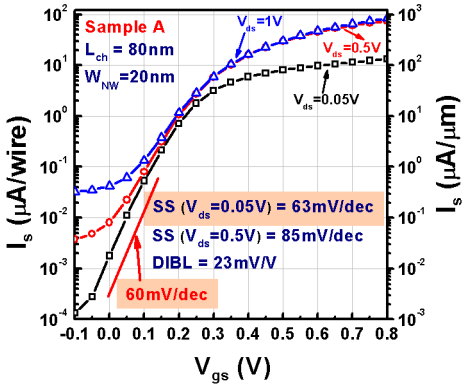


Fig. 10 Transfer characteristics of L_{ch}=80nm InGaAs GAA MOSFET (Sample A, W_{NW}=20nm) with SS=63mV/dec at V_{ds}=0.05V. Three measured devices show SS=63mV/dec.

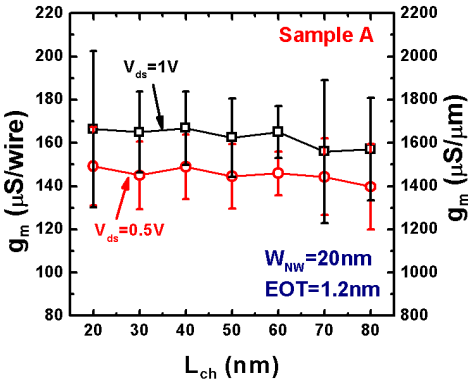


Fig. 11 g_m scaling metrics for sample A (EOT=1.2nm, W_{NW}=20nm) at V_{ds}=0.5V and 1V.

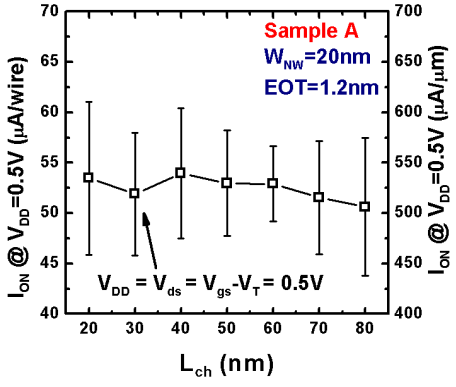


Fig. 12 I_{ON} scaling metrics for sample A (EOT=1.2nm, W_{NW}=20nm) at V_{ds}=V_{gs}-V_T=0.5V.

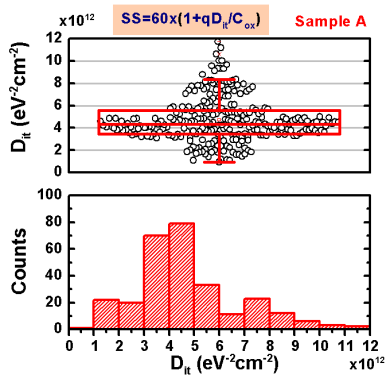


Fig. 13 Box plot and histogram for mid-gap D_{it} of sample A (W_{NW}=20-35nm, L_{ch}=50-80nm) extracted from SS. 3 devices have SS=63 mV/dec and 17 devices have SS<70 mV/dec.

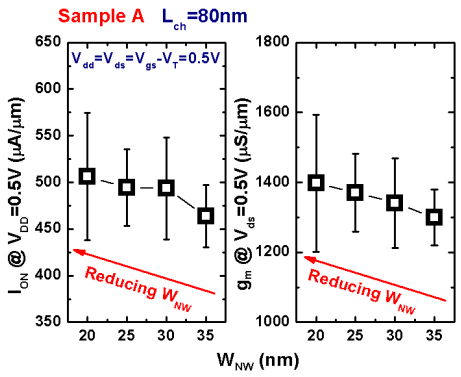
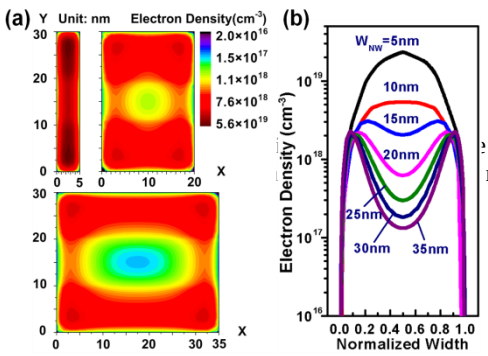


Fig. 14 W_{NW} dependence of the I_{ON} (V_{DD}=0.5V) and g_m (V_{ds}=0.5V), showing improved performance when reducing nanowire size.



measure

Fig. 15 (a) Simulated inversion charge distribution for current InGaAs nanowire MOSFETs with W_{NW}=5, 20, and 35nm, indicating volume inversion for all cases (b) Electron distribution along y=15nm for W_{NW}=5-35nm in 5nm step.

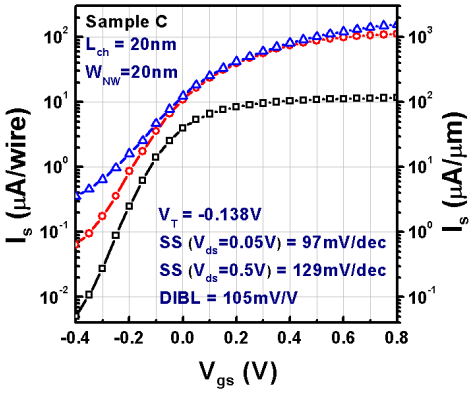


Fig. 16 Transfer characteristics of 20nm L_{ch} InGaAs GAA MOSFET with Al_2O_3 gate (Sample C, EOT=1.7nm) and W_{NW}=20nm.

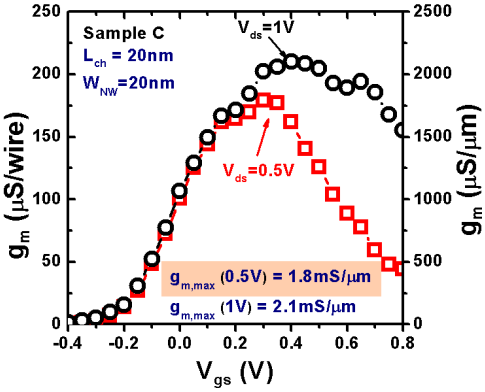


Fig. 17 Transconductance of 20nm L_{ch} InGaAs GAA MOSFET with Al_2O_3 gate (Sample C, EOT=1.7nm) and W_{NW}=20nm.

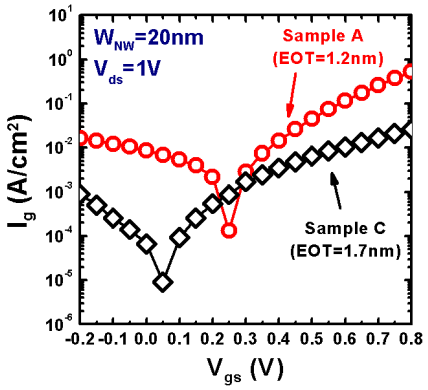


Fig. 18 Gate leakage of sample A (EOT=1.2nm) and sample C (EOT=1.7nm).

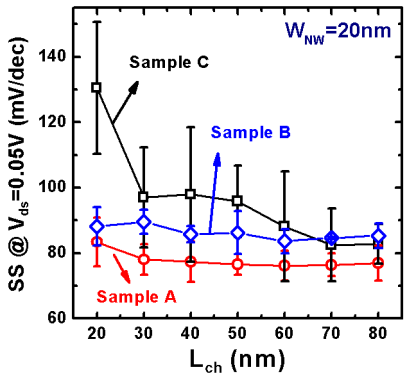


Fig. 19 DIBL scaling metrics for samples A, B, and C with W_{NW}=20nm.

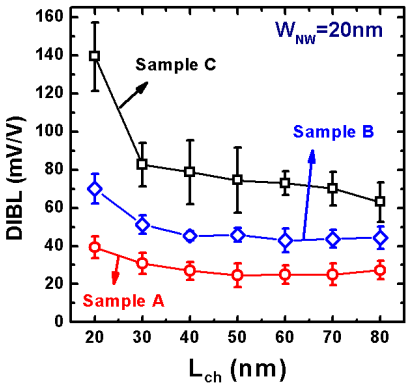


Fig. 20 SS scaling metrics for sample A, B, and C with W_{NW}=20nm.

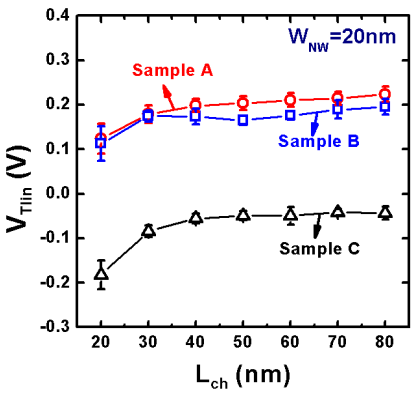


Fig. 21 V_T scaling metrics for sample A, B, and C with W_{NW}=20nm.

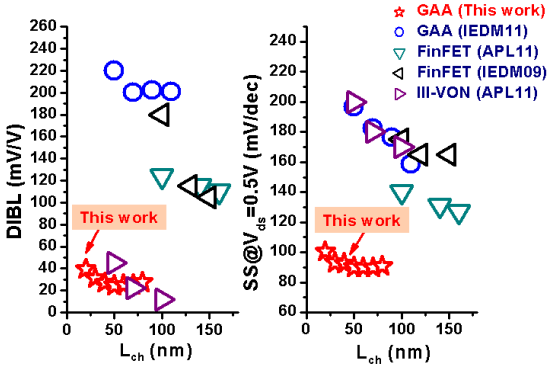


Fig. 22 SS/DIBL-L_{ch} benchmarking for InGaAs GAA nanowire MOSFETs in this work with InGaAs FinFETs, III-V-on-nothing nanowire MOSFETs, and InGaAs GAA MOSFETs demonstrated at Purdue.

Table 1: Performance benchmark of typical non-planar and ETB InGaAs MOSFETs

	This work**	Ref. [1]	Ref. [4]	Ref. [5]	Ref. [6]	Ref. [7]	Ref. [8]
$In_xGa_{1-x}As$ (x)	0.65	0.53	0.7	0.7	1	0.7	1
Structure	GAA	GAA	Tri-gate	GAA	GAA	FinFET	ETB
Fabrication	Top-down	Top-down	Top-down	Bottom-up	Bottom-up	Top-down	Top-down
$L_{ch\,(G)}$ (nm)	20	50	60	200	100	130	55
$W_{NW(Fin)}$ (nm)	20	30	30	90	15	220	-
EOT (nm)	1.2	4.5	1.2	1.8*	1.1*	4.5*	3.5
SS [V_{ds}=0.5V] (mV/dec)	88	245	94*	98	140	-	-
SS [V_{ds}=0.05V] (mV/dec)	63	145	66	90*	-	230*	105
DIBL (mV/V)	7	210	60*	170*	60	135	84
$g_{m,max}$ (mS/μm) [V_{ds}=0.5V]	1.65	0.45	-	-	1.23	-	-