III-V Gate-all-around Nanowire MOSFET Process Technology: From 3D to 4D

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Introduction: III-V gate-all-around (GAA) nanowire (NW) MOSFETs, or III-V 3D transistors, have been experimentally demonstrated by a top-down approach, showing excellent scalability down to channel length (L_{ch}) of 50nm [1]. However, the g_m, SS, and DIBL are greatly limited by the large EOT of the devices [1]. Furthermore, although lateral (parallel to the wafer surface) integration of NWs has been demonstrated with high drive current per wire, the overall current drivability of the devices is limited by the large pitch of the NWs. To overcome this drive current bottleneck, *for the first time*, a top-down process technology has been developed to fabricate vertically stacked (normal to the wafer surface) III-V NWFETs, similar to some explored Si NWFETs [2-3]. We call this new type of nanowire devices *III-V 4D transistors* to distinguish them from III-V 3D transistors [1] which has only one vertical layer and multiple lateral wires. The experimental results, in this abstract, show that the drive current per wire pitch (W_{pitch}) is greatly increased from 3D to 4D structure. The new device concept is very promising for future high-speed low-power logic and RF applications.

Experiments: Fig.1 shows the schematic diagram of III-V 3D and 4D transistors with 1×2 and 3×2 NW arrays respectively. The fabrication process for III-V 3D transistors is the same as in Ref. [1]. Fig. 2-3 shows the process flow and schematic diagram of key process steps for III-V 4D transistors. To achieve uniform source/drain doping to contact each of the three vertically stacked channel layers, a two-step Si implantation was performed at energies of 20keV and 60keV both with a dose of 1×10^{14} cm^{-2}. To enable the formation of InGaAs/InP fins with a fin height (H_{Fin}) of 200nm via reactive ion etching, ALD Al_2O_3 was used as a hard mask to replace the electron beam resist [1], providing excellent etching selectivity and eliminate resist redeposition. A new Cl_2/O_2 etching chemistry was developed replacing the BCl_3 based etching [1] to increase etch rate and improve sidewall quality. HCl-based solution was used to release the NW arrays patterned along [100] direction. Table 1 summarizes the splits for the NW array, NW size, EOT and Indium content of InGaAs. Fig. 4(a) shows a top-view SEM image of a III-V 4D transistor with 4 parallel NW stacks. Fig. 4(b) shows the fin test structure after Cl_2/O_2 dry etching. Fig. 4(c)-(d) show the cross sectional TEM images of InGaAs 3×1 and 3×4 NW arrays, showing that the ALD gate stack was coated around entire NW stacks. The ALD process of depositing highly conformal WN films for the gate metal is described in Ref [4]. The excellent step coverage of WN was examined on a sample of holes with 0.3 μm in diameter and 11 μm in depth (aspect ratio = 37:1). As shown in Fig. 5, the film thickness was 41 nm and 32 nm in the top and bottom zones, giving 78% step coverage on a 37 aspect ratio structure.

Results and discussion: Fig. 6-8 show the well-behaved output characteristics, transfer characteristics, and g_m-V_{gs} of a III-V 3D transistor (sample 1) with L_{ch}=50nm and W_{NW}=25nm. The current is normalized by the total perimeter of the NW, i.e. $W_G=2\times(W_{NW}+H_{NW})\times$(Wire Number). The I_{ON} reaches 1.2mA/μm at V_{ds}=1V and V_{gs}-V_T=1.2V, with maximum g_m=1.1mS/μm and 1.4mS/μm at V_{ds}=0.5V and 1V respectively. Good off-state performance is also achieved with SS=94mV/dec and DIBL=50mV/V. Fig. 9-11 show the DIBL, SS and V_T scaling metrics for sample 1 compared with sample 3 published in Ref. [1]. The 2× reduction in EOT greatly suppressed the short channel effects, evident by the dramatic reduction in DIBL, SS and the improvement in V_T roll off property. DIBL and SS are unchanged over the entire L_{ch} range and show little dependence on W_{NW}, indicating excellent gate electrostatic control. Fig. 12-13 show I_{on} and g_m scaling metrics for W_{NW}=25, 30, and 35nm. Gradual increase in on-state metrics are obtained due to shorter L_{ch}. Higher I_{ON} and g_m are obtained on devices with smaller W_{NW}, due to the volume inversion effect [5]. Fig. 14 shows the output characteristics of a L_{ch}=200nm 4D transistor with 3×4 NW array (sample 2). The I_{ON} reaches 1.35mA/μm at V_{ds}=1V and V_{gs}=2V normalized by perimeter. Maximum g_m of 0.6mS/μm and 0.85mS/μm are obtained at V_{ds}=0.5V and 1V respectively, as shown in Fig. 15. Fig. 16 shows the gate leakage current for sample 1, 2, and 3. Sample 2 (4D) shows similarly low leakage as sample 3 (3D), while sample 1 (3D) shows a slightly increased leakage due to the reduction of EOT. Further EOT scaling on both 3D and 4D structures is achievable. Fig. 17 depicts g_m-V_{gs} for III-V 4D transistors with 3×2 versus 3×4 NW arrays, showing increased drivability, e.g. I_{ON}, by adding NW stacks. To benchmark the overall current drivability for 3D and 4D technologies, I_{ON} and $g_{m,max}$ are normalized by W_{pitch}, defined as the maximum W_{NW} of the vertical NW stacks. For III-V 3D transistors, $W_{pitch}=W_{NW}$. The I_{ON}/W_{pitch} and g_m/W_{pitch} are figures of merit which evaluate the drivability per unit width along the plane of the wafer, as shown in Figs. 18-19. Sample 1 shows $2\times I_{ON}$ and $2.5\times g_m$ enhancement over sample 3 due to mobility enhancement and EOT scaling. Sample 2 shows additional $2\times I_{ON}$ and $1.5\times g_m$ enhancements over sample 1 due to the introduction of 4D structure despite the large EOT. Maximum I_{ON}/W_{pitch} and g_m/W_{pitch} reaches 9mA/μm and 6.2mS/μm for 4D FETs, which can be further improved by optimizing R_{SD} [6-9].

Conclusions: We have experimentally demonstrated, for the first time, III-V 4D transistor fabrication process using ALD. Electrostatic control has been improved and record high I_{ON}/W_{pitch} and g_m/W_{pitch} of 9mA/μm and 6.2mS/μm has been obtained for 4D transistors, showing 4× improvements over the III-V 3D transistors.

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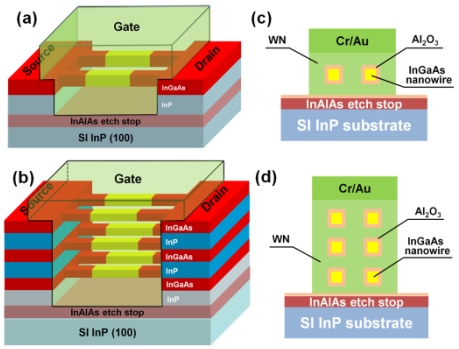


Fig. 1 Schematic diagram of III-V (a) 3D and (b) 4D transistors. (c) and (d) show the cross sectional views of the NWs for (a) and (b), showing 1×2 and 3×2 NW arrays, respectively.

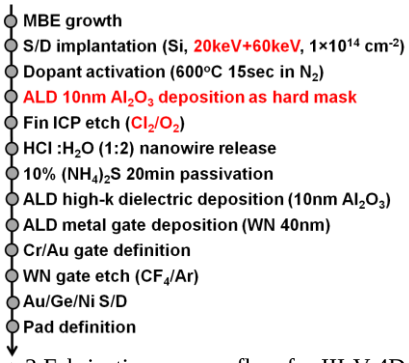


Fig. 2 Fabrication process flow for III-V 4D transistors with vertical and lateral integrations of InGaAs NWs. Novel process technologies in addition to those developed in Ref. [1] are highlighted in red.

Table 1 NW array (vertical×lateral), NW size and EOT splits for sample 1 and 2 fabricated in this work, and sample 3 in Ref. [1].

	Structure	NW Array (H×W)	Al_2O_3 Thickness (nm)	W_{NW} (nm)	H_{NW} (nm)	$In_xGa_{1-x}As$ (x)
Sample 1 (This work)	3D	1×4	5	25 30 35	30	65%
Sample 2 (This work)	4D	3×2 3×4	10	20 (Layer1) 60 (Layer2) 100 (Layer3)	30	53%
Sample 3 (IEDM11)	3D	1×1 1×4 1×9 1×19	10	30 50	30	53%

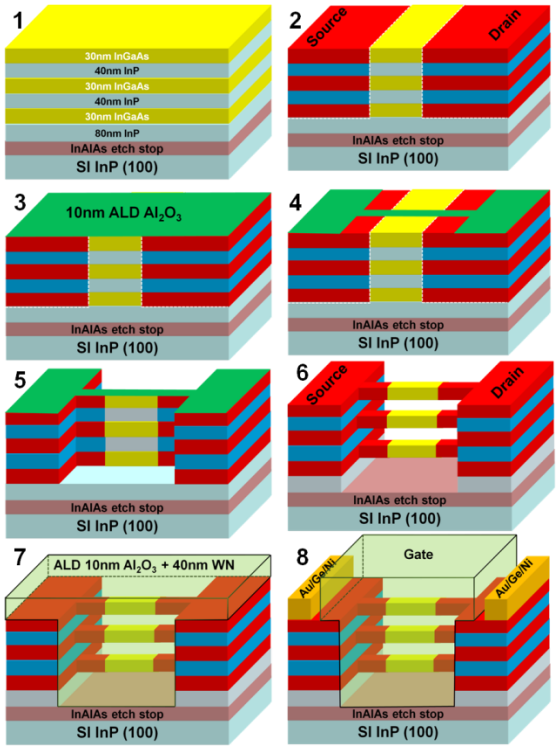


Fig. 3 Schematic diagram of key process steps in the fabrication of III-V 4D transistors with 3 layers of InGaAs NWs stacked vertically.

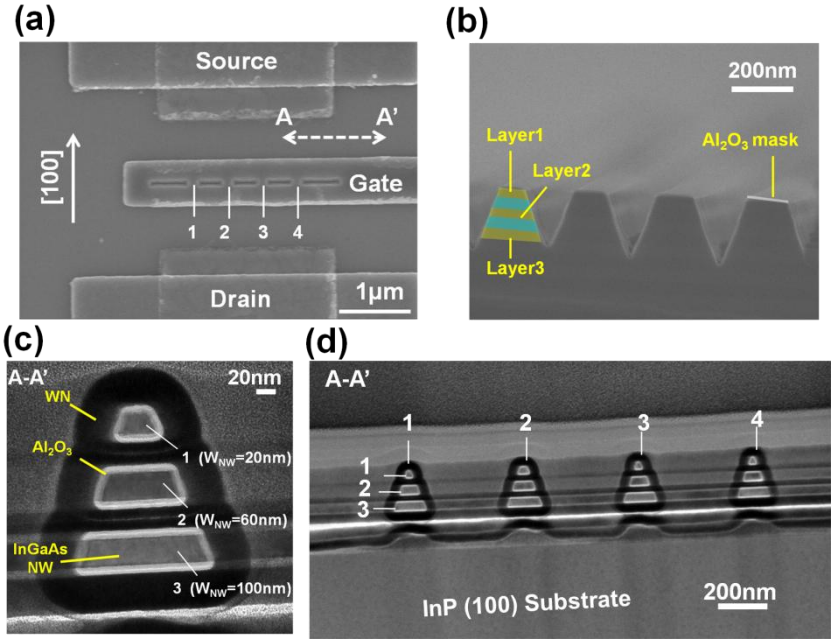


Fig. 4 (a) Top-view SEM image of a III-V 4D transistor with 4 parallel NW stacks. (b) Cross-sectional SEM image of InGaAs/InP fin test structures fabricated by Cl_2/O_2 dry etching with ALD Al_2O_3 as hard mask (c) Cross-sectional TEM image of a 3×1 InGaAs NW stack. The W_{NW} for layer 1, 2 and 3 is measured to be 20, 60, and 100nm. A better anisotropic dry etch process needs to be developed. The H_{NW} for each layer is 30nm defined by MBE. (d) Cross-sectional TEM image of the 3×4 NW array on a real device.

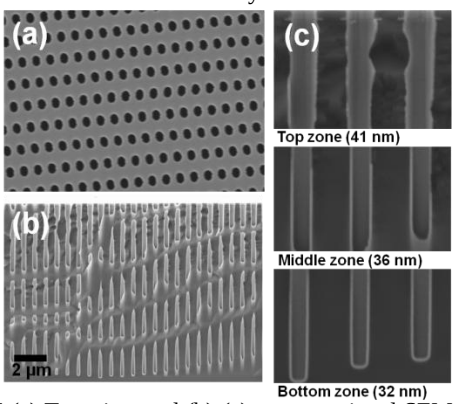


Fig. 5 (a) Top-view and (b)-(c) cross sectional SEM images of an ALD WN coated hole sample with an aspect ratio of 37:1. The film thickness of 41nm, 36nm, and 32nm was obtained in top, middle and bottom zones, indicating 78% step coverage. A superior conformal ALD WN process is critical in this III-V 4D transistor process.

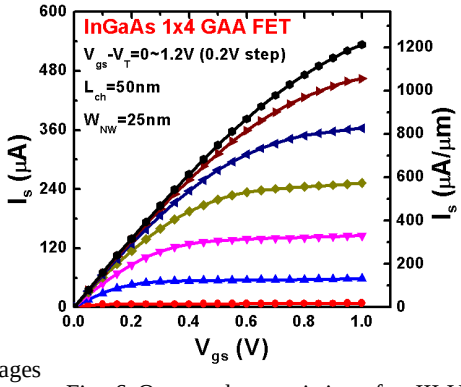


Fig. 6 Output characteristics of a III-V 3D FET with 1×4 NW array (sample 1). Current is normalized by the total perimeter of the NWs.

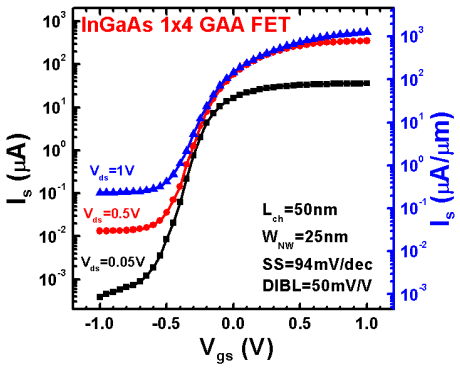


Fig. 7 Transfer characteristics of a III-V 3D FET with 1×4 NW array (sample 1).

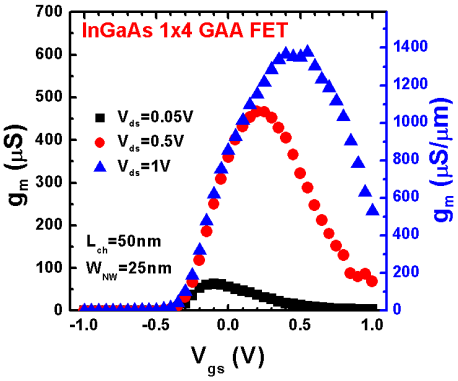


Fig. 8 g_m-V_{gs} of a III-V 3D FET with 1×4 NW array (sample 1).

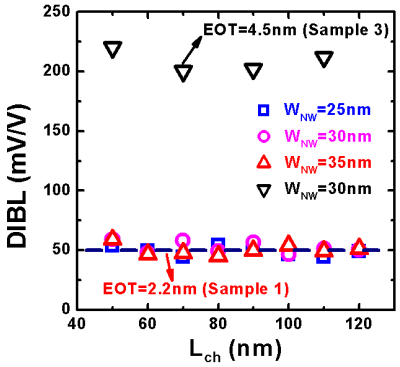


Fig. 9 DIBL scaling metrics for a III-V 3D FET with 1×4 NW array (sample 1) compared with sample 3 in Ref. [1].

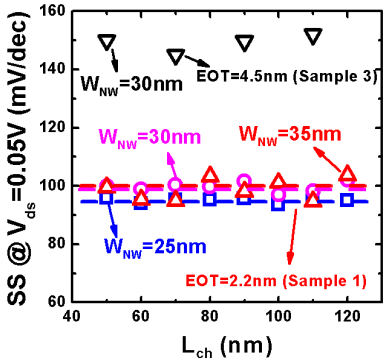


Fig. 10 SS scaling metrics for a III-V 3D FET with 1×4 NW array (sample 1) compared with sample 3 in Ref. [1].

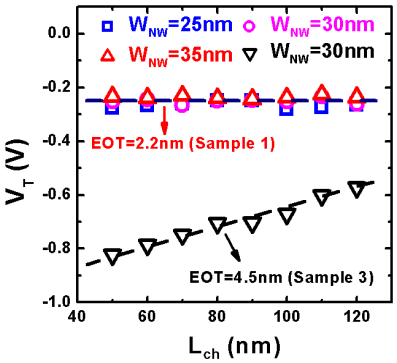


Fig. 11 V_T scaling metrics for a III-V 3D FET with 1×4 NW array (sample 1) compared with sample 3 in Ref. [1].

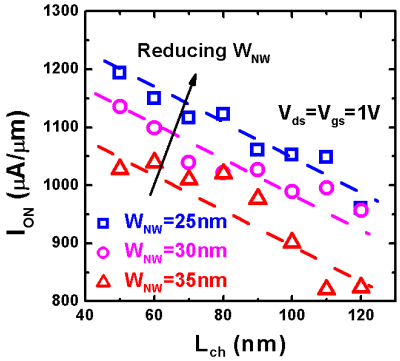


Fig. 12 I_{ON} scaling metrics for III-V 3D FETs with 1×4 NW arrays (sample 1), showing increased I_{ON} with reduced W_{NW}.

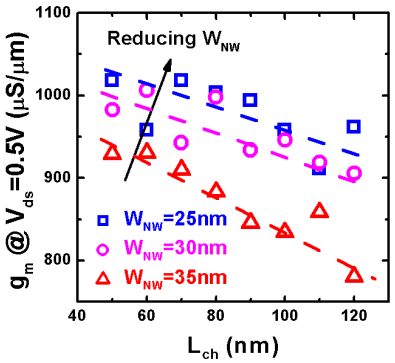


Fig. 13 g_m scaling metrics for III-V 3D FETs with 1×4 NW arrays (sample 1), showing increased g_m with reduced W_{NW}.

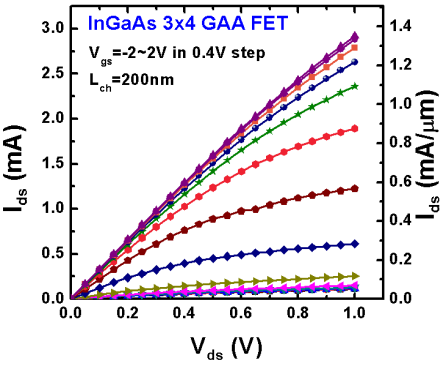


Fig. 14 Output characteristics of a III-V 4D FET with 3×4 NW array (sample 2). Current is normalized by the total perimeter of the NWs.

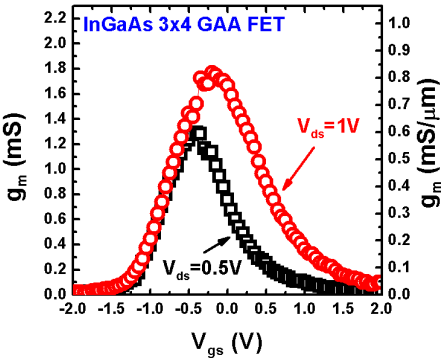


Fig. 15 g_m-V_{gs} of a III-V 4D FET with 3×4 NW array (sample 2).

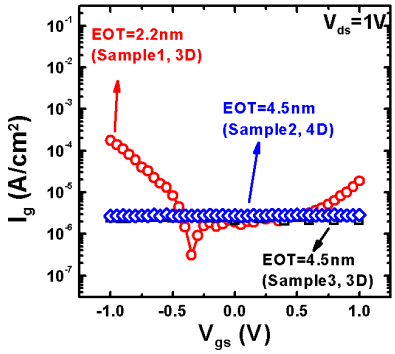


Fig. 16 Gate leakage current density for III-V 3D and 4D FETs (Sample 1, 2, and 3).

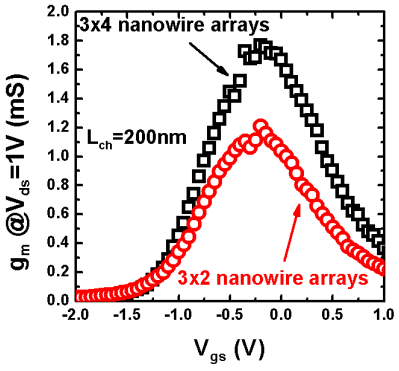


Fig. 17 g_m-V_{gs} of III-V 4D FETs with 3×2 and 3×4 NW arrays.

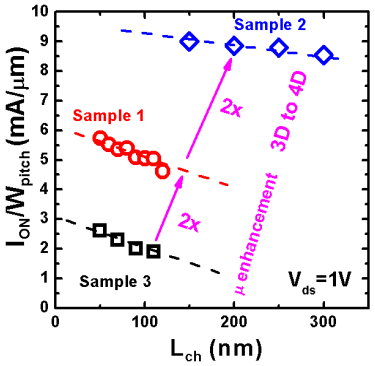


Fig. 18 Benchmarking I_{ON} per W_{pitch} for sample 1, 2, and 3, indicating the benefit of EOT scaling, mobility enhancement and vertical NW stacking from 3D to 4D integration.

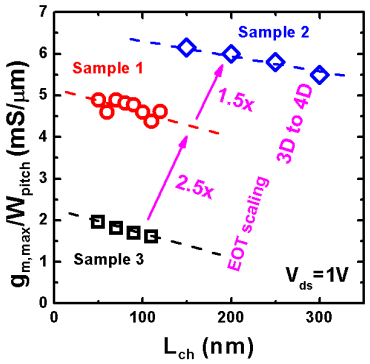


Fig. 19 Benchmarking g_m per W_{pitch} for sample 1, 2, and 3, indicating the benefit of EOT scaling, mobility enhancement and vertical NW stacking from 3D to 4D integration.